IN THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application.

Claim 1 (Currently Amended): A method for manufacturing a semiconductor device comprising:

forming a dummy gate electrode on a semiconductor substrate having a predetermined length coincident with a length of a gate electrode to be formed;

with the dummy gate electrode used as a mask, forming one pair of first impurity diffusion layers in regions of the semiconductor substrate which are opposite to each other on opposite sides of the dummy gate electrode;

forming an insulating film on the semiconductor substrate so as to ~~burry~~ bury the dummy gate electrode and exposing an upper surface of the dummy gate electrode;

removing the dummy gate electrode to form a first trench electrode in the insulating film having a width corresponding to at least the predetermined length of the dummy gate;

enlarging the width of the first trench on each side of the first trench by a predetermined amount to form a second trench in the insulating film using an etchant having an etching selectivity between the insulating film and the semiconductor substrate, said predetermined amount being equal to or greater than a thickness of a gate insulation film to be lined on an inner surface of the second trench;

lining the gate insulating film of said thickness along the inner surface of the second trench; and

forming the gate electrode in the second trench with only the gate insulating film intervening therebetween.

Claim 2 (Previously Presented): The method according to claim 1, further comprising:

after forming the first impurity diffusion layers, forming a side wall insulating film on a side wall surface of the dummy gate electrode; and

with the dummy gate electrode and the sidewall insulating film used as a mask, forming second impurity diffusion layers having a deeper junction in the semiconductor substrate than the first impurity diffusion layers.

Claim 3 (Previously Presented): The method according to claim 1, wherein the forming of a second trench includes performing an isotropic etching on the insulating film having the first trench formed therein.

Claim 4 (Canceled).

Claim 5 (Previously Presented): The method according to claim 1, wherein the forming of the gate insulating film includes using an insulating material having a relative dielectric constant of above 5.

Claim 6 (Previously Presented): The method according to claim 1, wherein the forming of a gate insulating film includes using an insulating material selected from the group consisting of Ta_2O_5, silicon nitride, Al_2O_3, $BaSrTiO_3$, Zr oxide, Hf oxide, Sc oxide, Y oxide and Ti oxide.

Claim 7 (Previously Presented): A method of manufacturing a semiconductor device, comprising:

forming a first insulating film on a semiconductor substrate;

sequentially forming a first semiconductor film and a second insulating film on the first insulating film;

forming a resist pattern on the second insulating film;

with the resist pattern used as a mask, patterning the first semiconductor film and the second insulating film by an anisotropic etching to provide a stacked layer structure of the first semiconductor film and the second insulating film on the semiconductor substrate having a predetermined width coincident with a length of a gate electrode to be formed;

with the stacked layer structure used as a mask, ion-implanting an impurity in the semiconductor substrate to provide first impurity diffusion layers for a source and a drain;

forming a third insulating film over the semiconductor structure to bury the stacked layer structure;

etching back the third insulating film to expose an upper surface of the stacked layer structure;

with the third insulating film used as a mask, removing the stacked layer structure to form a trench in the third insulating film;

after forming the trench, enlarging the width of the trench by an isotropic etching by a predetermined width amount on each side of the trench that is equal to or larger than a thickness of a fourth insulating film along an inner surface of the trench using an etchant having an etching selectivity between the insulating film and the semiconductor substrate;

after enlarging the width of the trench, depositing the fourth insulating film of said thickness along the inner surface of the trench; and

forming a conductive layer on and in contact with the fourth insulating film to form said gate electrode of a length coincident with the predetermined width.

Claim 8 (Previously Presented): The method according to claim 7, further comprising:

after providing the first impurity diffusion layers, forming a sidewall insulating film on a sidewall of the stacked layer structure; and

with the sidewall insulating film and the staked layer structure used as a mask, forming second impurity diffusion layers having a deeper junction in the semiconductor substrate than the first impurity diffusion layers.

Claim 9 (Previously Presented): The method according to claim 7, wherein the enlarging of the width of the trench includes using, as the isotropic etching, an etching treatment including HF or NH_4F.

Claim 10 (Previously Presented): The method according to claim 7, wherein the depositing of the fourth insulating film includes depositing by a chemical vapor deposition method or a sputtering method.

Claim 11 (Canceled).

Claim 12 (Previously Presented): The method according to claim 7, wherein the depositing of the fourth insulating film includes using an insulating material having a dielectric constant of above 5.

Claim 13 (Previously Presented) The method according to claim 7, wherein the depositing of the fourth insulating film includes using an insulating material selected from the

group consisting of Ta_2O_5, silicon nitride, Al_2O_3, $BaSrTiO_3$, Zr oxide, Hf oxide, Sc oxide, Y oxide and Ti oxide.

Claim 14 (Withdrawn): A semiconductor device comprising:

a semiconductor substrate;

a first impurity diffusion layer formed in the semiconductor substrate;

a second impurity diffusion layer formed in the semiconductor substrate in a spaced-apart relation to the first impurity diffusion layer;

a first insulating layer formed on the first impurity diffusion layer;

a second insulating layer formed on the second impurity diffusion layer;

a trench formed over the semiconductor substrate in a manner to be defined between the first insulting layer and the second insulating layer;

a gate insulating film lined on a bottom surface and an inner sidewall surface of the trench; and

a gate electrode formed in the trench with the gate insulting film intervening therebetween, the gate electrode being formed in an overlapped relation relative to the first impurity diffusion layer and the second impurity diffusion layer.

Claim 15 (Withdrawn): The semiconductor device according to claim 14, wherein the gate insulting film is formed of an insulting material having a dielectric constant of above 5.

Claim 16 (Withdrawn): The semiconductor device according to claim 14, wherein the gate insulating film contains one selected from the group consisting of Ta_2O_5, silicon nitride,

Al_2O_3, $BaSrTiO_3$, Zr oxide, Hf oxide, Sc oxide, Y oxide, and Ti oxide.

Claim 17 (Withdrawn): The semiconductor device according to claim 14, wherein the first impurity diffusion layer and the second impurity diffusion layer, each, comprise a third impurity diffusion layer including a portion formed beneath the gate insulating film formed on the inner sidewall surface of the trench and a fourth impurity diffusion layer including a portion formed beneath any of the first insulating layer and second insulating layer and having a deeper junction in the semiconductor substrate than the third impurity diffusion layer.

Claim 18 (Withdrawn): The semiconductor device according to claim 14, further comprising a metal silicide layer formed on the first impurity diffusion layer and the second impurity diffusion layer at those areas beneath the first insulating layer and the second insulating layer.